INSTALLATION MANUAL

ACC-84E

(EnDat 2.2)

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EnDat 2.2 (HEIDAINHAIN)

May 20, 2011

INTRODUCTION

ACC-84E(Universal serial encoder interface) 와 EnDat 2.2 (HEIDAINHAIN) 프로토콜의 Encoder 와의 설정 방법에 대해서 설명을 하겠습니다.

Global Control Register

Global register 는 Clock 과 피드백 프로코콜의 트리거 설정을 합니다. 해당 Base Register + $F 이며, X-word 입니다. 아래의 표는 각 카드의 Address 에 따른 Switch 설정 입니다.

Base Address	Global Control Register	Switch Position (SW1)			
		1	2	3	4
$78C00	X:$78C0F	Close	Close	Close	Close
$79C00	X:$79C0F	Close	Close	Open	Close
$7AC00	X:$7AC0F	Close	Close	Close	Open
$7BC00	X:$7BC0F	Close	Close	Open	Open
$78D00	X:$78D0F	Open	Close	Close	Close
$79D00	X:$79D0F	Open	Close	Open	Close
$7AD00	X:$7AD0F	Open	Close	Close	Open
$7BD00	X:$7BD0F	Open	Close	Open	Open
$78E00	X:$78E0F	Close	Open	Close	Close
$79E00	X:$79E0F	Close	Open	Open	Close
$7AE00	X:$7AE0F	Close	Open	Close	Open
$7BE00	X:$7BE0F	Close	Open	Open	Open

아래의 표는 해당 Register 의 각 Bit 별 기능 설명입니다.

Bit Description of Global Register Located at X-Word Base Address + $F																							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M Divisor								N Divisor				Reserved		Trigger Clock	Trigger Edge	Trigger Delay				Protocol code			

Bit	Type	Default	Name	Description
[23:16]	R/W	$00	M_Divisor	Intermediate clock frequency for *SER_Clock*. The Intermediate clock is generated from a (M+1) divisor Clocked at 100 Mhz.
[15:12]	R/W	$2	N_Divisor	Final clock frequency for *SER_Clock*. The final clock is Generated from a 2^N divisor clocked by the intermediate Clock.
[11:10]	R	$0	Reserved	Reserved and always reads zero.
[09]	R/W	$0	TriggerClock	Trigger clock select for initiating serial encoder communications: 0 = PhaseClock 1 = ServoClock
[08]	R/W	$0	TriggerEdge	Active clock egde select for the trigger clock: 0 = rising edge 1 = falling edge

[07:04]	R/W	$0	TriggerDelay	Trigger delay program relative to the active edge of the trigger clock. Units are in increments of 20 usec.
[03:00]	R	$3	ProtocolCode	This read-only bit field is used to read the serial encoder Interface protocol supported by the FPGA. A value of $3 define this protocol EnDat 2.2.

Bit 12 부터 Bit 23 까지는 Serial Encoder 로 보내지는 Clock 설정에 대한 계산 수식입니다.

$$\text{Clock Frequency} = \frac{100}{25 \times (M+1) \times 2^{N}} \text{ MHz}$$

M	N	Clock Frequency
0	2	1.0 MHz*
0	3	500 KHz
0	4	250 KHz
* Default Setting for 1 MHz transfer rates		

각 Channel 의 해당하는 Control Register

각각의 채널에 해당하는 control register 가 있으며, 해당하는 Bit 들의 해당하는 각각의 기능을 설정/비설정하는 역할을 합니다.

Bit Description of Channel Specific Control Register
Channel 1 : X:Base + $0 Channel 2 : X:Base + $4 Channel 3 : X:Base + $8 Channel 4 : X:$Base + $C

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		Command Code						Reserved		Trigger Mode	Trigger Enable	Reserved	RxData Ready/ SENC	Reserved				Position Bits					

Bit	Type	Default	Name	Description
[23:22]	R	$0	Reserved	Reserved and always reads zero.
[21:16]	R	$0	Command Code	Command transmitted to the encoder. Valid settings are: 000111 – Encoder to Send Position (EnDat 2.1 & 2.2) 101010 – Encoder to Receive Reset (EnDat 2.1 & 2.2) 111000 – Encoder to Send Position (EnDat 2.2 only) 101101 – Encoder to Receive Reset (EnDat 2.2 only)
[15:14]	R	$0	Reserved	Reserved and always reads zero.
[13]	R/W	$0	Trigger Mode	Trigger Mode to initiate communication: 0 = continuous trigger 1 = one – shot trigger All trigger occur at the defined Phase/Servo clock edge and delay setting. See Global Control register for these setting

[12]	R/W	$0	Trigger Enable	Enable trigger for serial encoder communications: 0 = disabled 1 = enabled This bit must be set for either trigger mode. If the Trigger Mode bit is set for one-shot mode, the hardware Will automatically clear this bit after the trigger occurs.
[11]	R/W	$0	reserved	Reserved and always reads zero.
[10]	R	$3	ProtocolCode	This read-only bit field is used to read the serial encoder Interface protocol supported by the FPGA. A value of $3 define this protocol EnDat 2.2.
	W	$0	SEN_MODE	This write-only bit is used to enable the output drivers for the SENC_SDO, SENC_CLK, SENC_ENA pins for each Respective channel. It also directly drives the respective SENC_MODE pin for each channel.
[09:06]	R	$0	Reserved	Reserved and always reads zero.
[05:00]	W	$0	Position Bits	This bit field is used to define the number of position data bits or encoder resolution : Range is 12 – 40 (001100 – 101000)

명령 코드 [21:16] 은 아래와 같은 4 가지 통신 모드를 지원합니다.

- EnDat 2.1 mode, Encoder to send position value (000111)
- EnDat 2.1 mode, Encoder to receive reset (000111)
- EnDat 2.2 mode, Encoder to send position value (111000)
- EnDat 2.2 mode, Encoder to receive reset (101101)

Position Data Register

각 채널에 해당하는 위지 데이터는 각채널의 Control register 의 24-bit Y-word 에 저장됩니다.

각 Encoder 의 위지 데이터는 SerialEncoderDataA 에 저장되며 오버플로우 bit 들은 SerialEncoderDataB 에 저장됩니다.

Channel	Data Register A	Data Register B
1	Y:Base + $0	Y:Base + $1
2	Y:Base + $4	Y:Base + $5
3	Y:Base + $8	Y:Base + $9
4	Y:Base + $C	Y:Base + $D

Serial Encoder Data Register A																						
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
First 24 bits of position data																							

Serial Encoder Data Register B																						
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Timeout Error	CRC Error	Encoder Error Flag	Reserved									Upper 12 bits of position data											

SerialEncoerDataB 의 상위 3Bit 는 Error 에 해당하는 내용을 나타내며, 리셋 명령으로 재 설정이 가능합니다. CRC_Error 는 되받은 Data 의 CRC 비교 실패이며, Timrout Error flag 는 Encoder 의 응답을 받지 못한 상태를 나타냅니다.

EnDat 2.2 Feedback Setup Example:

Encoder : HEIDAINHAIN Encoder (Resolution :1nm) 를 사용하며, 극간 거리 36mm 인 Linear 모터의 Direct PWM 전용 앰프 설정 예제 입니다.

-Terminal window

```
WX:$78C00, $002003          ; Global Control register, 1MHz clock setting, EnDat 2.2
WX:$78C00, $071424          ; Ch1 Control register, 36-Bit EnDat Encoder
```

- Encoder Conversition Table

```
I8000 = $278C00             ; Unfilrered parallel position of location
I8001 = $018000             ; 24-bit processed result at $3502
I103 = $3502                ; Position loop feedback address
I104 = $3502                ; velocity loop feedback address
I108 = 1                    ; Resolution 이 높기 때문에 지령 속도 계산을 위함
I109 = 1                    ; Resolution 이 높기 때문에 지령 속도 계산을 위함
```

- 초기화 PLC 1 설정

```
Open plc 1 clear
Disable plc 2..31
cmd"wx:$78C0F, $002003"     ; Global Control register, 1MHz Clock setting, Endat 2.2
cmd"wx:$78C00, $71424       ; Channel 1, read 36 bits
Disable plc 1
Enable plc 2..31
Close
```

● Commutation 을 위한 극간 간격에 해당하는 Ixx70, Ixx71, Ixx83 설정

- Ixx83 (Commutation Position Address)설정

```
I8002 = $2F8C00
```

I8003 = $010008 ; Read 16bits

Ixx83 = @I8003

모터 극간 거리 36mm 이며, mm/cts 는 36000000cts 입니다.

이에 따라 Ixx70, Ixx71 을 설정해야 하나 Ixx71 파라메터의 범위가 0~16777215 이므로 Phase search 를 위한 Encoder 의 Resolution 을 줄여서 설정해야합니다.

36000000 / 256 = 140625 ; 16 Bit phase cycle count

Ixx70 = 1

Ixx71 = 140625

● EnDat 2.2 Absolute Encoder Position 초기화 PLC

원활한 튜닝을 위한 제어 Resolution 을 8nm 로 설정함

- 초기화 PLC 설정

```
Y:$78C00,0,24,U         ; Position Data A (Lower) ->     24Bit
Y:$78C01,0,16,U         ; Position Data B (High)->       12Bit

#define ENDAT_POS_LOW           M4002
#define ENDAT_POS_HIGH          M4003
#define ORIGIN                  P5000

M4002->Y:$78C00,0,24,U      ; Position Register Low
M4003->Y:$78C01,0,16,U      ; Position Register High

open plc2 clear
I5111=(1000)*838608/I10
While (I5111 > 0)
EndWhile

//Endat pos. high
P4003=M4003 & $FFF          ; Register 12Bit Mask ($FFF)
P4004=M4002/8               ; 8 Bit shift (해당 Resolution 이 너무 높아 줄임)

// Positive Encoder Data
```

```
If (P4003 < $800)
//  ORIGIN =( (P4003 * $1000000 + P4004)*(I108*32) )
M162 = ( (P4003 * $1000000 + P4004)*(I108*32) )
Else
;Negaive Encoder Data
  P4002 = M4002 ^ $FFFFFF     ; 2'보수 계산을 위함
  P4006 = P4002 / 8                   ; 3 Bit shift
  P4004 = P4003 ^ $FFF
  M162=-(P4004*$100000+P4002+1)*(I108*32)
EndIf

dis plc2
close

/// Error check
M4005->Y:$78C01,0,24,U
P4005=M4005 & $E00000
```